CLAIMS

WE CLAIM:

1. A method of testing a memory under test on a memory tester, the method comprising the steps of:

(a) applying the same sequence of transmit vectors to the memory under test and to a work memory within the memory tester, the sequence of transmit vectors causing the storing of test pattern data within the memories to which it is applied; and

(b) subsequent to step (a), comparing the test pattern data content of the memory under test with the test pattern data content of the work memory.

2. A method as in claim 1 wherein the same sequence of transmit vectors is an instance of that sequence that is applied simultaneously to the memory under test and to the work memory.

3. A method as in claim 1 wherein the same sequence of transmit vectors is separate instances of that sequence that are applied at different times to the memory under test and to the work memory.

4. A method as in claim 1 wherein the work memory is a selectable portion of an interior test memory within the memory tester.

5. A method as in claim 4 further comprising the step of interleaving work memory transactions among banks of DRAM.

6. A method as in claim 4 further comprising the step of storing comparison results from step (b) in an error catch memory that is a portion of an interior test memory within the tester.

7. A method as in claim 6 further comprising the step of interleaving error catch memory transactions among banks of DRAM.

8. A method as in claim 4 wherein the interior test memory is comprised of a plurality of memory sets and the selectable portion is a segment of a memory set.

9. A method as in claim 8 further comprising the step of storing comparison results from step (b) in an error catch memory that is a portion of a memory set different than the memory set of which the work memory is a segment.